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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,893	10/02/2003	Robert C. Chang	SANDP040	2329

10027 7590 01/18/2006

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,893	CHANG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15,17-25,27-32 and 34-45* is/are rejected.

7)☒ Claim(s) *6,16,26 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03,05/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-45 are presented for examination in this application (10,678,893) filed on October 2, 2003.

Acknowledgement is made to the Information Disclosure Statement received on October 27, 2003 and May 14, 2004.

The original claims 30-46 have been renumbered as claims 29-45 by the Applicants per their preliminary amendment filed on 10/02/2003.

Claim Objections

According to the preliminary amendment filed on 10/02/2003, original claims 30-46 have been renumbered as claims 29-45 due to the missing of claim 29 in the original disclosure. However, the wording of each claim has not been amended accordingly to reflect the renumbering of the claims. For example, the claim presently numbered as 29 (originally claim 30) now recites "the memory system of claim **29**," instead of "the memory system of claim **28**."

Claims presently numbered as 29-45 need to be updated to indicate their correct dependency.

For the subsequent claim analysis in this Office Action, the claim number is referred to by the new, presently numbered sequence.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 11-12, 21-22, 28-29, 35, 38-39 and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams et al. (US Patent Application Publication 2001/0042230).

As to claim 1, Williams et al. disclose **a method** [Sector Validation for Use in ECC Engine Validation (title)] **for storing data within a non-volatile memory** [data to be stored in a physical sector of a disk drive (figure 2, 108; abstract), and a disk drive is a non-volatile memory] **of a memory system** [figure 2], **the method comprising**:

identifying a first block into which the data is to be stored [the method includes choosing a physical sector (i.e., a first block) to use for running a validation test for validating the ECC engine (abstract; figure 4, step 402)];

obtaining an indicator associated with the first block [the host computer (figure 2, 200) sends commands specifying a physical sector to which data is to be written (paragraphs 0030, 0034 and 0038); the commands includes an indication as to whether to send the data block directly to the disk (figure 2, 108; i.e. to bypass ECC encoding) or to send the data block to the ECC calculating module (figure 3, 304) (paragraph 0034); the host sends an indicator to the disc drive that the disc drive should disable ECC (paragraph 0041)];

determining when the indicator indicates that the data is to be encoded using a first algorithm [the host sends an indicator to the disc drive that the disc drive should disable ECC (paragraph 0041); the write decision module (figure 3, 302) uses the

command to determine whether to send the data block directly to the disk (figure 2, 108; i.e. to bypass ECC encoding) or to send the data block to the ECC calculating module (figure 3, 304) (paragraph 0034); the ECC algorithm may be Reed-Solomon codes (paragraphs 0004~0006)];

encoding the data using the first algorithm when it is determined that the data is to be encoded using the first algorithm [if the write decision module 302 determines to send the data block to the calculating module 304, the calculating module 304 receives the data block and calculates an ECC for the data block (paragraph 0035)]; **and**

writing the data encoded using the first algorithm into the first block [figure 3; paragraph 0035].

As to claim 2, Williams et al. teach that **encoding the data using a second algorithm** [the second algorithm is to bypass/disable the ECC all together (figure 3; paragraph 0035)], **when it is determined that the data is not to be encoded using the first algorithm** [paragraphs 0034-0035]; **and**

writing the data encoded using the second algorithm into the first block [figure 3; paragraph 0034].

As to claim 11, refer to "As to claim 1."

As to claim 12, refer to "As to claim 2."

As to claim 21, refer to "As to claim 1."

As to claim 22, refer to "As to claim 2."

As to claim 28, refer to "As to claim 1."

As to claim 29, refer to "As to claim 2."

As to claim 35, refer to "As to claim 1." Further, Williams et al. teach that a disc drive having discs with some good physical sectors (i.e., first block) and some bad physical sectors (i.e., second block) [paragraph 0058], and that a good sector is indicated by the disable of the ECC encoding/decoding function and a bad sector would have the ECC encoding/decoding function enabled [paragraph 0054]. The data structure associated with whether the first or the second ECC algorithm is used is the calculated ECC data [paragraph 0035]. If the ECC encoding/decoding function is enabled, the calculated ECC data would be appended to the data block in the target sector, and If the ECC encoding/decoding function is disabled, no calculated ECC data would be present [paragraph 0035].

As to claim 38, refer to "As to claim 1."

As to claim 39, refer to "As to claim 2."

As to claim 42, refer to "As to claim 1."

As to claim 43, refer to "As to claim 2."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 13, 23, 30, 36, 40 and 44 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams et al. (US Patent Application Publication 2001/0042230), and in view of Applicants' admission of prior art.

As to claims 3, 13, 23, 30, 36, 40 and 44, the two ECC algorithms mentioned by Williams et al. is a Reed-Solomon algorithm (paragraphs 0004~0006), which is a 2-bit ECC algorithm, and an ECC bypassing algorithm. Thus Williams et al. do not explicitly mention the 1-bit ECC algorithm.

However, Applicants admit in the "Background of the Invention" section of their disclosure that both the 1-bit and 2-bit ECC algorithms are well known in the art (paragraph 0009).

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that both the 1-bit and 2-bit ECC algorithms are well known in the art, as admitted by Applicants, hence lacking patentable significance.

6. Claims 9-10, 19-20, 27, 34, 37, 41 and 45 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams et al. (US Patent Application Publication 2001/0042230), and in view of Kramer (US 6,182,239).

As to claims 9-10, 19-20, 27, 34, 37, 41 and 45, Williams et al. do not mention that **the non-volatile memory is a flash memory, and particularly, one of a NAND flash memory and an MLC NAND flash memory.**

However, the invention of Williams et al. is directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

7. Claims 4-5, 19-20, 37, 41 and 45 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams et al. (US Patent Application Publication 2001/0042230), and in view of Bruce et al. (US 5,956,743).

As to claim 4, Williams et al. do not teach that the indicator is arranged to indicate when the block is a reclaimed block.

However, Bruce et al. teach in their invention "Transparent Management at Host Interface of Flash-memory Overhead-Bytes Using Flash-Specific DMA Having Programmable Processor-Interrupt of High-Level Operations" a block management and replacement scheme for wear0leveling using ECC as part of the overhead bytes in a flash-memory chips [abstract] in which dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) [column 1, lines 57-67].

Using erase/write counters as indicators to support wear-leveling operations increases the life expectancy of a non-volatile memory device such as flash memory chip.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that benefit of using erase/write counters as indicators to support wear-leveling operation, as demonstrated Bruce et al., and to incorporate it into the existing scheme disclosed by Williams et al. to further improve the life expectancy of the non-volatile memory devices.

As to claim 5, Bruce et al. teach that **the indicator is arranged to indicate a number of times the block has been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 7, Bruce et al. teach that **the indicator is arranged to indicate an approximately average number of times blocks within the non-volatile memory have been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 8, Bruce et al. teach that **the indicator is stored in a data structure, the data structure being substantially separate from the first block, and obtaining the indicator associated with the block includes obtaining the indicator from the data structure** [the data structure is the dual write counters that are allocated

to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

As to claim 17, refer to "As to claim 7."

As to claim 18, refer to "As to claim 8."

As to claim 24, refer to "As to claim 4."

As to claim 25, refer to "As to claim 5."

As to claim 31, refer to "As to claim 4."

As to claim 32, refer to "As to claim 5."

Allowable Subject Matter

8. Claims 6, 16, 26 and 33, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Blake et al., (US 5,228,046), "Fault Tolerant Computer memory Systems and Components Employing Dual Level error Correction and Detection with Disablement Feature."
- Bruce et al., (US 6,000,006), "Unified Re-Map and Cache-Index Table with Dual Write-Counters for Wear-Leveling of Non-Volatile Flash RAM Mass Storage."

- Stuart Fiske et al., (US 6,487,685), "system and Method for Minimizing Error Correction code Bits in Variable Sized Data Formats."
- Mokhlesi, (US Patent Application Publication 2004/0228197), "Compressed Event Counting Technique and Application to a Flash Memory System."
- Sukegawa et al., (US 5,603,001), "Semiconductor Disk System Having a Plurality of Flash memories."
- Takahashi, (US Patent Application Publication 2002/0008928), "Magnetic Disc Device and Error Correction Method Therefor."
- Bruce et al., (US 6,970,890), "Method and Apparatus for Data Recovery."
- Estakhri et al., (US Patent Application Publication 2001/0029564), "Identification and Verification of a Sector within a Block of Mass Storage Flash Memory."

Conclusion

10. Claims 1-5, 7-15, 17-25, 27-32 and 34-45 are rejected as explained above.

Claims 6, 16, 26 and 33, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 27, 2005

PIERRE BATAILLE
PRIMARY EXAMINER
1\12\06